
HD74LV1GT126A

Bus Buffer Gate with 3–state Output

HITACHI

ADE-205-333B (Z)
3rd. Edition
April 2000

Description

The HD74LV1GT126A has a bus buffer gate with 3–state output in a 5 pin package. Output is disabled when the associated output enable (OE) input is low. To ensure the high impedance state during power up or power down, OE should be connected to V_{CC} through a pull-down resistor; the minimum value of the resistor is determined by the current sourcing capability of the driver. Low voltage and high speed operation is suitable for the battery powered products (e.g., notebook computers), and the low power consumption extends the battery life.

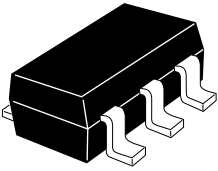
Features

- The basic gate function is lined up as hitachi uni logic series.
- Supplied on emboss taping for high speed automatic mounting.
- TTL compatible input level.
Supply voltage range : 4.5 to 5.5 V
Operating temperature range : -40 to $+85^{\circ}\text{C}$
- All inputs V_{IH} (Max.) = 5.5 V (@ $V_{CC} = 0$ V to 5.5 V)
All outputs V_O (Max.) = 5.5 V (@ $V_{CC} = 0$ V)
- Output current ± 12 mA (@ $V_{CC} = 4.5$ V to 5.5 V)
- All the logical input has hysteresis voltage for the slow transition.

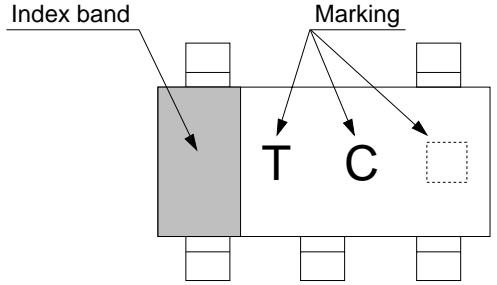
HD74LV1GT126A

Outline and Article Indication

- HD74LV1GT126A



CMPAK-5



□ = Control code
(— or blank)

Function Table

Inputs		Output Y
OE	A	
H	H	H
H	L	L
L	X	Z

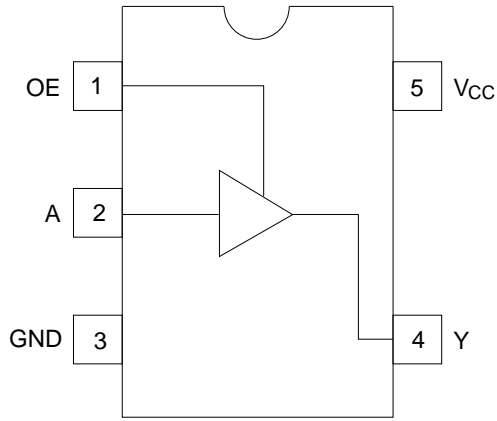
H : High level

L : Low level

X : Immaterial

Z : High impedance

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Test Conditions
Supply voltage	V_{CC}	-0.5 to 7.0	V	
Input voltage	V_{IN}	-0.5 to 7.0	V	
Output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$ -0.5 to 7.0	V	Output : H or L V_{CC} : OFF
Input diode current	I_{IK}	-20	mA	
Output diode current	I_{OK}	± 50	mA	
Output current	I_{OUT}	± 25	mA	
V_{CC} , GND current	I_{CC} or I_{GND}	± 50	mA	
Power dissipation	P_T	200	mW	
Storage temperature	T_{stg}	-65 to 150	°C	

Recommended Operating Conditions

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	4.5 to 5.5	V
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to +85	°C
Input rise / fall time	t_r, t_f	0 to 20 ($V_{CC} = 4.5$ to 5.5 V)	ns

Electrical Characteristic

- $T_a = -40$ to 85°C

Item	Symbol	V_{CC} (V) *	Min	Typ	Max	Unit	Test condition
Input voltage	V_{IH}	4.5 to 5.5	2.0	—	—	V	
	V_{IL}	4.5 to 5.5	—	—	0.8		
Hysteresis voltage	V_H	5.0	—	0.15	—	V	$V_T^+ - V_T^-$
Output voltage	V_{OH}	Min to Max	$V_{CC}-0.1$	—	—	V	$I_{OH} = -50 \mu\text{A}$
		4.5	3.8	—	—		$I_{OH} = -12 \text{ mA}$
	V_{OL}	Min to Max	—	—	0.1		$I_{OL} = 50 \mu\text{A}$
		4.5	—	—	0.55		$I_{OL} = 12 \text{ mA}$
Input current	I_{IN}	0 to 5.5	—	—	± 1	μA	$V_{IN} = 5.5 \text{ V}$ or GND
Quiescent supply current	I_{CC}	5.5	—	—	10	μA	$V_{IN} = V_{CC}$ or GND, $I_O = 0$
	ΔI_{CC}	5.5	—	—	1.5	mA	One input $V_{IN} = 3.4 \text{ V}$, other input V_{CC} or GND
Output leakage current	I_{OFF}	0	—	—	5	μA	$V_O = 5.5 \text{ V}$
Input capacitance	C_{IN}	5.0	—	3.0	—	pF	$V_{IN} = V_{CC}$ or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

- $V_{CC} = 5.0 \pm 0.5$ V

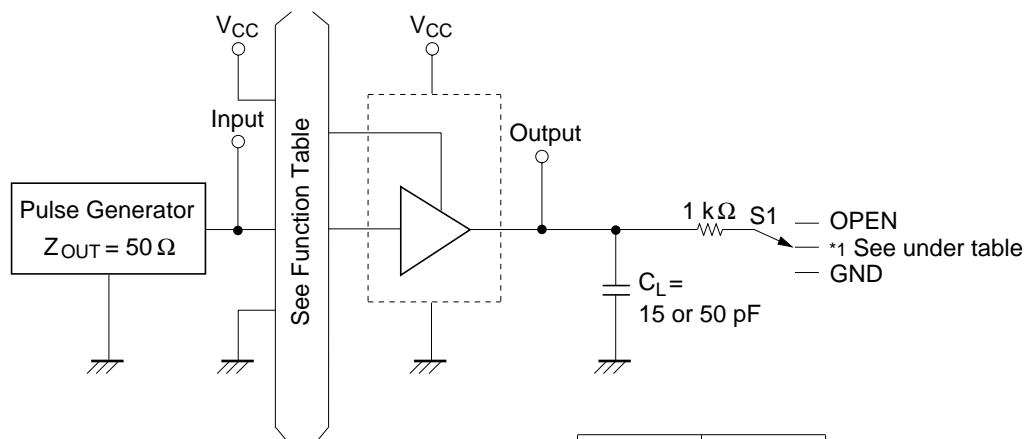
Item	Symbol	$T_a = 25^\circ\text{C}$			$T_a = -40$ to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t_{PLH}	—	3.5	5.5	1.0	6.5	ns	$C_L = 15$ pF	A	Y
	t_{PHL}	—	4.6	7.5	1.0	8.5		$C_L = 50$ pF		
Enable time	t_{ZH}	—	3.6	5.1	1.0	6.0	ns	$C_L = 15$ pF	OE	Y
	t_{ZL}	—	4.6	7.1	1.0	8.0		$C_L = 50$ pF		
Disable time	t_{HZ}	—	3.3	6.8	1.0	8.0	ns	$C_L = 15$ pF	OE	Y
	t_{LZ}	—	4.3	8.8	1.0	10.0		$C_L = 50$ pF		

Operating Characteristics

- $C_L = 50$ pF

Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			Unit	Test Conditions
			Min	Typ	Max		
Power dissipation capacitance	C_{PD}	5.0	—	11.5	—	pF	$f = 10$ MHz

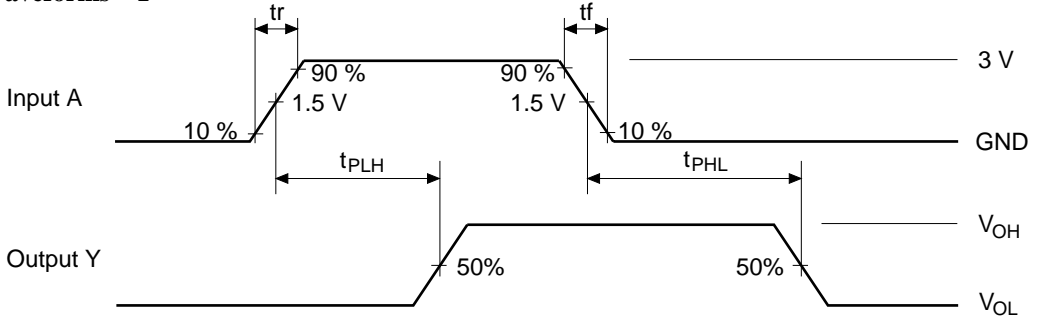
Test Circuit



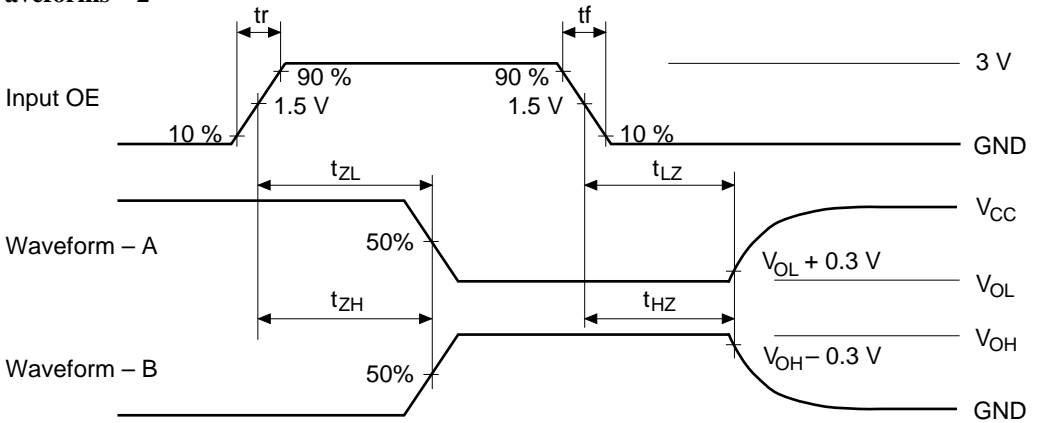
TEST	S1
t_{PLH} / t_{PHL}	OPEN
t_{ZH} / t_{HZ}	GND
t_{ZL} / t_{LZ}	V _{CC}

Note: 1. C_L includes probe and jig capacitance.

• Waveforms – 1



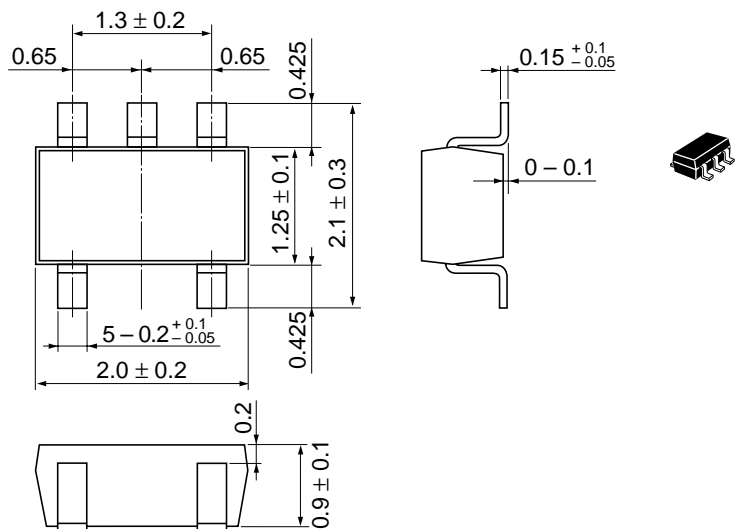
• Waveforms – 2



- Notes:
1. $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$
 2. Input waveform : $\text{PRR} \leq 1 \text{ MHz}$, duty cycle 50%
 3. Waveform – A is for an output with internal conditions such that the output is low except when disabled by the output control.
 4. Waveform – B is for an output with internal conditions such that the output is high except when disabled by the output control.

Package Dimensions

Unit : mm



Hitachi Code	CMPAK-5
JEDEC	—
EIAJ	—
Weight (reference value)	0.006 g

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